IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	
	)	
Michael N. Derr for	)	
Intel Corporation	)	
	)	
Serial No.: 09/821,116	)	Group Art Unit: 2142
	)	
Filed: March 30, 2001	)	Examiner: PRITO, BEATRIZ

For: **Bit-Granular Writes of Control Registers**

REPLY BRIEF IN SUPPORT OF APPELLANT'S APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant hereby replies to the Examiner's Answer dated March 8, 2007.

Filed EFS-WEB on May 8, 2007

Status of claims:

Claims 2, 3 and 5-25 are pending. Claims 1 and 4 have been cancelled. Claims 2, 3 and 5-25 are the subject of the appeal.

The Examiner has maintained rejection of the claims 2, 3 and 5-25.

All of the arguments in Appellant's Appeal Brief ("Appeal Brief"), filed on September 27, 2006 are herein incorporated into this Reply Brief to the Examiner's Answer.

Before responding to the arguments provided in the Examiner's Answer, it is respectfully submitted that several technical aspects of the Examiner's Answer remain inaccurate and problematic.

The examiner has presumed obviousness based on the teachings of the combination of Baker (US patent no. 5996032) and Runaldue (US patent no. 5999441). As is well established, Appellant submits that a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the modifications, as presumed by the Examiner, *See Gillette Co. v. S.C. Johnson & Son, Inc.* 919 F. 2d 720 (Fed Cir. 1990).

In the Examiner's Answer, the Examiner appears to attempt to combine the teachings of Runaldue, of an application using random access memory for storing data having multiple configuration length with the teachings of Baker, of an environment including PC cards and memory cards, e.g., a SRAM card and ROM card using IEEE 1394 standard communication typically used for communication via telephone lines.

Appellant submits that Runaldue discloses memory architecture, for example, random access memory (RAM) configured to store a prescribed number of words

having a predetermined word length. Such RAM structures, known as word organized arrays, have a prescribed number of columns and rows. The RAM has a prescribed number of bits defining a word length including memory cells that enable selective overwriting on bit-by-bit basis.

The Examiner appears to equate the memory architecture of Runaldue with the controller as required by the Appellant's claimed invention to receive a data value of a write directed to a control register of the controller and interpreting bits of the data value as a data field, the number of bits in the data field being equal to the number of bits in the control register of the controller and bit locations in the data field corresponding respectively to bit locations in the control register.

Appellant submits that a person skilled in the art would not consider the memory architecture and its functioning of Runaldue similar to the controller and it's functioning of the Appellant's invention. Therefore, writing a memory, having a prescribed number of bits defining a word length including memory cells that enable selective overwriting on bit-by-bit basis disclosed by Runaldue does not appear to be similar to the Appellant's invention.

Appellant further believes that the Examiner has erroneously presumed that the register write circuitry 250 and it's functioning, as disclosed by Baker, is similar to the controller and it's functioning as required by the Appellant's invention. Baker discloses that in the register write circuitry 250, general purpose I/O (GPIO) write data input 252 is received by data flip flop 254. The data flip flop 254 also receives clock signal 256 and write enable input 258 from AND function 260. AND function 260 receives GPIO address okay signal 262, write strobe standard signal 264, and GPIO address bit input

266. AND function 260 provides the AND output 258 to write enable bit 268 of data flip flop 250. Only flip flop 250 with a 1 in particularly assigned address bit 266 will be written with the respective GPIO write data 252. Baker appears to disclose that the register write circuitry 250 permits writing only to bits that must change in a register, while preserving the previous value of the remainder of the bits.

Appellant submits that a person skilled in the art would not consider the register write circuitry of Baker similar to the Appellant's controller, which requires receiving a data value of a write directed to a control register of the controller and interpreting bits of the data value as a data field, the number of bits in the data field being equal to the number of bits in the control register of the controller and bit locations in the data field corresponding respectively to bit locations in the control register. Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

Appellant submits that there appears to be no suggestion or motivation for one skilled in the art to combine the references. Therefore, a prima facie case of obviousness has not been established, as presumed by the Examiner. Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

Appellant now addresses the new arguments put forth, by the Examiner in the Examiner's Answer to the Appellant's Appeal Brief, with regard to the rejected claims.

The Examiner rejected claims 2-3, 5-21 under 35 USC 102(e) as being unpatentable over Baker (US patent no. 5996032) and Runaldue (US patent no. 5999441).

Appellant respectfully submits that claim 12 requires receiving a data value of a write directed to a control register in the controller and interpreting bits of the data value as a data field and as enable bits in bit enable field and the number of bits being equal to the number of bits in the control register.

In column 3, lines 15-27, Baker discloses a method and system for writing a plurality of data register bits. The method and system include storing both designation address bits in an address field for addressing a predetermined data register. The designation address bit designates predetermined bits within the data register to which the data is to be written as active and other bits within the data register as inactive.

Thus, Baker includes writing data only to the predetermined bits within the data register using single write command. However, Appellant is unable to locate where Baker teaches receiving a data value of a write directed to a control register and interpreting bits of the data value as a data field and as enable bits in bit enable field and the number of bits being equal to the number of bits in the control register, by the controller, as required by Appellant's claim 12. Instead, Appellant believes that the controller of the Appellant's invention being provided between said device and said processor subsystem.

In FIG. 1 and column 3, lines 30-57, Runaldue illustrates a block diagram of a random access memory (RAM). The RAM 10 is composed of an array of memory cells 12 arranged in eight columns 14 (C0 – C7), where a column is a 128 by 1-bit array of SRAM cells. The RAM 10 also includes an address decoder 16 and a bit enable decoder logic 18. The RAM 10 may operate as a conventional memory, where each bit of the input data (0:7) is written into corresponding column array 14 at a selected raw

specified by a corresponding one of the word line (WORDLN) and in response to write enable signal (WE).

Further, in column 3, line 65 to column 4, line 5, column 5, lines 28-29, and column 1, lines 19-41, Runaldue discloses that the bit enable decoder logic 18 may output a unique bit enable signal to each column array 14 to enable writing to an addressed word on a bit-by-bit basis. The decoder logic 18 may output the same bit enable signal to a selected group of columns to provide variable-width memories, for example converting an 8-bit wide RAM to two 4-bit memory array, or 2-bit memory array. Further, Runaldue, discloses that the decoder 62 can be configured to configure the RAM as a full 8-bit wide RAM if mask equals 1 to assert all the bit enable signals for all the columns. Runaldue also discloses that memory architecture are typically configured to store a prescribed number of words having a predetermined word length. Such memory structures, known as word organized arrays, have a prescribed number of columns and rows.

In column 2, lines 7-12 and 20-32, Runaldue discloses that a bit selectable mask enables each bit of data input to be selectively written into a corresponding memory cell, where the memory cell includes a logic circuit for selectively overwriting a stored value based on the corresponding bit of the mask. Thus, Runaldue appears to disclose the low level details of a random access memory (RAM) array which can be written at the bit level. Runaldue neither discloses the bus level protocol (that is bit enable enclosed in the data phase) nor a system in which control register are written.

Therefore, Appellant is unable to locate where Runaldue teaches receiving a data value of a write directed to a control register in the controller and interpreting bits of

the data value as a data field and as enable bits in bit enable field and the number of bits being equal to the number of bits in the control register, as required by the Appellant's claim 12.

Further, Appellant submits that Runaldue discloses a memory architecture having a bit enable decoder logic 18 which may output a unique bit enable signal to each column array 14 to enable writing to an addressed word on a bit-by-bit basis.

Appellant submits that a person skilled in the art would not consider the memory architecture of Runaldue similar to the controller having a control register of the Appellant's invention and therefore the write operation of Runaldue, to write memory, appears to be different than the write operation as required by the controller of the Appellant's invention of claims 12. Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

Further, the examiner, in the response to the arguments section of the Examiner's answer, states that Baker teaches receiving a data value of a write directed to a register. Appellant submits that Baker, in Fig. 10 and related description, teaches that in the register write circuitry 250, general purpose I/O (GPIO) write data input 252 is received by data flip flop 254. The data flip flop 254 also receives clock signal 256 and write enable input 258 from AND function 260. AND function 260 receives GPIO address okay signal 262, write strobe standard signal 264, and GPIO address bit input 266. AND function 260 provides the AND output 258 to write enable bit 268 of data flip flop 250. Only flip flop 250 with a 1 in particularly assigned address bit 266 will be written with the respective GPIO write data 252. Thus, Baker appears to disclose that the register write circuitry 250 permits writing only to bits that must change in a register,

while preserving the previous value of the remainder of the bits. Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

Further, the Examiner's Answer states that the specification does not seem to mention FIG. 4. The Appellant submits that FIG. 4 has been described in paragraph [0034], as amended, at the time of attending to the First Office Action. The Appellant invites kind attention of the learned Examiner to paragraph [0034].

As is well established, Appellant submits that a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the modifications proposed by the Examiner, *See Gillette Co. v. S.C. Johnson & Son, Inc.* 919 F. 2d 720 (Fed Cir. 1990).

The Examiner's Answer appears to attempt to combine the teachings of Runaldue, "using random access memory for storing data having multiple configuration length" with the teachings of Baker, "environment including PC cards. Appellant submits that the combination does not arrive at the Appellant's invention of claim 12 as the combination does not teach receiving a data value of a write directed to a control register and interpreting bits of the data value as a data field and as enable bits in bit enable field and the number of bits being equal to the number of bits in the control register, as required by the Appellant's claim 12.

Appellant submits that, in the light of the above arguments, there appears to be no suggestion or motivation for one skilled in the art to combine the references. Therefore, a prima facie case of obviousness in regard to claim 12 has not been established. Appellant respectfully requests that the rejection of claim 12 be reversed.

Appellant respectfully submits that claims 13-14 include claim 12 as a base claim. Accordingly, claims 13-14 are allowable for at least the reasons stated above in regard to claim 12. Appellant believes the above reasons are sufficient to overcome the present rejection of claims 13-14 under Baker and Runaldue. Appellant respectfully requests that the rejection of claims 13-14 be reversed.

Appellant respectfully submits that claim 15 include claim 12 as a base claim. Accordingly, claim 15 is allowable for at least the reasons stated above in regard to claim 12. Moreover, claim 15 requires the processor subsystem posts an entire command sequence in the controller for setting up the IDE (integrated drive electronics) data transfer.

The Examiner's Answer states that Baker discloses that the PCI-interface ASIC (20 of FIG. 1) performs a primary function of controlling transfer of data packets between devices operating in an environment that supports PCI bus 24 and devices operating in a high-speed input/output peripheral environment (column 5, lines 40 - 44 (not column 5, lines 15-34 as indicated by the Examiner)). Further, in FIG. 2, Baker shows a general functional partitioning of PCI-interface ASIC 20 as per his invention. Also, in column 20, lines 41 - 49, Baker discloses that PCI-interface ASIC 20 can issue write command on PCI bus 24 by specifying the appropriate address range in the controlling packet control list.

The Examiner appears to equate the PCI interface 20 of Baker with the processor subsystem of the Appellant's invention. Appellant submits that the processor subsystem may comprise existing hardware associated with the register of the controller (see paragraph 0034) and as required by the Appellant's claim 10. On the contrary,

Baker discloses a PCI interface provided between the PCI and the peripheral devices. Appellant submits that a person skilled in the art would not consider the PCI interface of Baker similar to the processor subsystem of the Appellant's claim 10. Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

Also, Runaldue does not appear to teach that the processor subsystem posts an entire command sequence in the controller for setting up the IDE data transfer, as required by the Appellant's claim 15. Appellant submits that neither Runaldue nor Baker appear to teach that the processor subsystem posts an entire command sequence in the controller for setting up the IDE (integrated drive electronics) data transfer. Appellants therefore respectfully disagrees with the position of the Examiner and requests that the rejection of claim 15 be reversed.

Appellant submits that claim 16 requires overwriting only the bits at the bit locations of the register for which a corresponding enable bit in the data value is set with corresponding data bits in the data value. The Examiner's Answer has made the rationale of rejection regarding claim 20 (as claim 1 has been cancelled) applicable to the claim 16. Appellant therefore submits that the arguments submitted in regard to claims 20 appears to be relevant to claim 16. Further, Appellant is unable to locate where Baker teaches overwriting only the bits at the bit locations of the register of controller for which a corresponding enable bit in the data value is set with corresponding data bits in the data value.

Also, Runaldue teaches an arrangement for enabling data to be written in an addressed word in memory on bit-by-bit basis, but does not teach overwriting only the

bits at the bit locations of the register for which a corresponding enable bit in the data value is set with corresponding data bits in the data value.

Appellant submits that neither Baker nor Runaldue teach overwriting only the bits at the bit locations of the register for which a corresponding enable bit in the data value is set with corresponding data bits in the data value. The proposed combination does not arrive at the invention of Appellant's claim 16. Appellant respectfully requests the rejection of claim 16 be reversed.

Appellant submits that claims 17-19 include claim 16 as a base claim. Accordingly, claims 17-19 are allowable for at least the reasons stated above in regard to claim 16. Further, the office action has made applicable the rationale of rejection regarding claims 2-3 and 9-10 applicable to the claims 17-19. Appellant therefore submits that the arguments submitted herein above in regard to claims 2-3 and 9-10 appears to be relevant to the claims 17-19. Appellant respectfully requests the rejection of claims 17-19 be reversed.

Appellant submits that claim 20 requires receiving data of a single write command comprising a bit enable field and a data field and each field comprises same number of bits.

The Examiner's Answer states that the write enable bit field 258 and the write input data field 252 are illustrated as input signals each as ONE bit value inputted to register write circuitry (i.e. write command operation). This circuitry shows <u>one</u> of an arbitrary number of similar circuits, each controlling a particular <u>bits</u> out of the arbitrary number or data bits. Appellant submits that Baker teaches that the register write circuitry 250 comprise a data flip-flop 250 to receive the GPIO write data input 252,

clock signal 256 and write enable input 258 (from AND function 260). Baker also teaches that when the write enable 268 is active, input write data 252 is written to flip flop 254 and appears on flip-flop output 270.

Appellant submits that the GPIO write data 252 and write enable bit 258 are received by the flip-flop 254 from two different sources that is from I/O controller as GPIO write data and AND functions as AND gate output, separately. Therefore, Appellant submits that a person skilled in the art would not treat, GPIO write data 252 and write enable bit 258, of Baker similar to the data of a single write command comprising a bit enable field and a data field and each field comprises same number of bits, as required by Appellant's claim 20. Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

In column 5, lines 11-21, Runaldue discloses implementation of bit enable decoder logic 18 wherein bit enable signal supplied to each of column 14 may be arranged with different decoding logic depending on the on the application. The Examiner's Answer states that FIG 3 illustrates a decoder 60 that posses each bit of the 8-bit mask signal, to a corresponding one of the columns 14 to provide a bit-by-bit mask writing capability. Thus, Runaldue appears to teach a bit enabled decoder logic 18 to enable bit by bit writing using data bits and mask bits, but there is no indication that the mask bits are part of the data bits transmitted in a write command. Further, Runaldue appears to be silent regarding how exactly the mask bits are transmitted. Runaldue thus does not teach receiving data of a single write command wherein the data comprises a bit enable field and a data field having same number of bits in each field, as required by the Appellant's claim 20.

The Examiner's Answer states, Runaldue, in column 2, lines 51-56, teaches that a single write operation comprising a data field (DATA [0:7]) and a bit enable mask field (BIT_EN [0:7]), where the bit enable filed and the data field the same number of bits. However, Appellant is unable where Runaldue teaches receiving data of a single write command wherein the data comprises a bit enable field and a data field having same number of bits in each field, as required by the Appellant's claim 20.

Further, the Examiner's Answer states that Runaldue (in column 2, lines 25-32, and lines 36-56) discloses that the logic circuit selectively cause to overwrite a stored value based upon the write signal and the corresponding bit enable signal. Also, the logic gate for generating a gating signal in response to a supplied write signal and a bit enable signal, the gating signal causing the corresponding memory cell. Appellant submits that Runaldue discloses that the logic circuit selectively cause the bistable latch to overwrite a stored value based upon the write signal and the corresponding bit enable signal. Hence, random access memory can be fabricated, where word based addressing can be used to access a selected memory location, while using a mask signal to write selected bit in the address memory word, without overwriting unselected bits of the addressed word. Runaldue further discloses that each memory cell including a logic gate for generating a gating signal in response to a supplied write signal and a bit enable signal. However, Appellant is unable to locate where Runaldue discloses receiving data of a single write command comprising a bit enable field and a data field and each field comprises same number of bits, as required by Appellant's claim 20. Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

Appellant submits that the proposed combination of Baker and Runaldue does not teach receiving data of a write command comprising a bit enable field and a data field comprises same number of bits and therefore the proposed combination does not arrive at the Appellant's invention of claims 20. Appellant respectfully requests the rejection of claim 20 be reversed.

Appellant submits that claims 2, 3 and 5 include claim 20 as a base claim. Accordingly, claims 2, 3 and 5 are allowable for at least the reasons stated above in regard to claim 20. Appellant submits that the above submissions are sufficient to overcome the present rejection of claims 2, 3 and 5 under Baker and Runaldue. Appellant respectfully requests that the rejection of claims 2, 3 and 5 be reversed.

Appellant submits that claim 6 includes claim 20 as a base claim. Accordingly, claim 6 is allowable for at least the reasons stated above in regard to claim 20. Moreover, claim 6 requires some of the bits of said register are not overwritten.

In column 2, lines 3-7, Runaldue discloses that there is a need for an arrangement enabling selected bits of data word to be selectively written into a random access memory without overwriting other non-selected bits of the data word stored in the memory. The Examiner appears to equate, "non-selected bits of data word stored in the memory" of Runaldue with "some of the bits of said register (control register)" of Appellant's claim 6. Appellant submits that one skilled in the art would not equate, "non-selected bits of data word stored in the memory" of Runaldue with "some of the bits of said register (control register)" of Appellant's claim 6, as the "bits of data word stored in the memory" of the Runaldue appear to be different than the "bits of the control register", because the memory do not appear to be similar to the control register.

Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

Further, Baker discloses a method where part of the address field is used to specify the bits to be loaded. However, Baker does not appear to teach that some of the bits of said register are not overwritten as required by the Appellant's claim 6.

Appellant submits that the proposed combination of Baker and Runaldue does not teach some of the bits of said register are not overwritten as required by the Appellant's claim 6, and therefore the proposed combination does not arrive at the Appellant's invention of claim 6. Appellant respectfully requests the rejection of claim 6 be reversed.

Appellant submits that claims 7-8 include claim 20 as a base claim. Accordingly, claims 7-8 are allowable for at least the reasons stated above in regard to claim 20. Moreover, claims 7 and 8 require data field and the bit enable field are received simultaneously and at respective address contiguous to each other.

The Examiner in the Examiner's Answer states that Runaldue, in column 4, lines 45-54 and FIG-2, discloses that simultaneous assertion of the write enable and bit enable signal causes the NAND gate 52 to output a "0". The bistable latch can then store data supplied on the data input line once the nodes N1 and N2 are connected to VCC and ground respectively. Appellant submits that as per the Appellant's invention the register (control register) receives data packet containing the bit enabled field and data field. On the contrary, as per Runaldue's invention the memory asserts write enable and bit enable signal as separate signals. Appellant submits that person skilled in the art would not consider separate assertion of the data field and the bit enable field

similar to the reception of data field and the bit enable field simultaneously and at respective address contiguous to each other, as required by Appellant's claim 7 and 8.

The Examiner's Answer states that Baker teaches writing data only to predetermined bits in a register write operation using a single write enable command. Specifically, the logic 64 implements the control required for the interface 20 to operate on PCI bus 24, which permits the operation of the memory writes instructions. For the memory write operation, the interface 20 DMA write operation results in a PCI memory write, memory write line command on the PCI bus (Column 7, lines 12-22). The PCI slave logic 66 performs the control logic necessary for PCI-interface ASIC 20 to operate on the PCI bus as a slave device (Column 7, lines 22-32). Appellant submits that Baker discloses a method where part of the address field is used to specify the bits to be loaded. However, Appellant is unable to locate where Baker teaches that data field and the bit enable field are received simultaneously and at respective address contiguous to each other, as required by the Appellant's claims 7 and 8. Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

Appellant submits that the proposed combination of Baker and Runaldue does not teach that the data field and the bit enable field are received simultaneously and at respective address contiguous to each other, as required by the Appellant's claims 7-8, and therefore the proposed combination does not arrive at the Appellant's invention of claims 7-8. Appellant respectfully requests the rejection of claims 7-8 be reversed.

Appellant submits that claims 9 - 11 include claim 20 as a base claim. Accordingly, claims 9 - 11 are allowable for at least the reasons stated above in regard

to claim 20. Moreover, claim 10 requires the processor subsystem to post the entire command sequence for setting up the data transfer.

The Examiner in the Examiner's Answer states that Baker discloses that the PCI-interface ASIC (20 of FIG. 1) performs a primary function of controlling transfer of data packets between devices operating in an environment that supports PCI bus 24 and devices operating in a high-speed input/output peripheral environment (column 5, lines 40 - 44 (not column 5, lines 15-34 as indicated by the Examiner)). Further, in FIG. 2, Baker shows a general functional partitioning of PCI-interface ASIC 20 as per his invention. Also, in column 20, lines 41 - 49, Baker discloses that PCI-interface ASIC 20 can issue write command on PCI bus 24 by specifying the appropriate address range in the controlling packet control list.

Appellant submits that the Examiner appear to equate the PCI interface 20 of Baker with the processor subsystem of the Appellant's invention. Appellant submits that the processor subsystem may comprise existing hardware associated with the register of the controller (see paragraph 0034) and as required by the Appellant's claim 10. On the contrary, Baker discloses a PCI interface provided between the PCI and the peripheral devices. Appellant submits that a person skilled in the art would not consider the PCI interface of Baker similar to the processor subsystem of the Appellant's claim 10. Appellant therefore respectfully disagrees with the position of the Examiner and requests that the rejection be reversed.

Further, Runaldue does not appear to teach the processor subsystem to post the entire command sequence for setting up the data transfer, s required by the Appellant's claim 10.

Appellant submits that neither Baker nor Runaldu appear to teach the processor subsystem as required by the Appellant's claim 10. Appellant further submits that even the combination of Runaldue and Baker does not anticipate the invention of the claim 10 of the Appellant. Appellant respectfully requests the rejection of claims 9-11 be reversed.

CONCLUSION

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

Date: May 8, 2007

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